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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,009	12/21/2001	Paul E. Doucette	004578.1147	2368

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EXAMINER	
BAYARD, EMMANUEL	
ART UNIT	**PAPER NUMBER**
2638	

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/028,009	DOUCETTE ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2638	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is in response to amendment filed on 6/20/05 in which claims 1-28 are pending. The applicant's amendments have been fully considered but they are moot based on the new ground of rejection.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-15, 20-26are rejected under 35 U.S.C. 102(e) as being anticipated by Obayashi et al U.S. patent No 6,249,249 B1.

As per claims 1, 7, 20, 23 Obayashi et al teaches an apparatus, comprising: first section (see figs.4, 15, 24-25, 27-28 element 113, 113b 213) which outputs first and second digital signals, said first digital signal representing a predetermined waveform with a first phase shift imparted thereto in relation to reference, said second digital signal representing substantially said predetermined waveform with second phase shift imparted thereto relation to said reference, said second phase shift being different from said first phase shift (see col.6, lines 1-35 and col.21, lines 40-65); digital-to-analog converter section which converts said first and second digital signals respectively into

first and second analog signals (see elements 123, 122, 232 and col.6, lines 36-67 and col.21, lines 56-63) phase shift section which produces a first adjusted signal by imparting to said first analog signal a phase shift which is substantially equal and opposite said first phase shift, and which produces second adjusted signal by imparting to said second analog signal a phase shift which substantially equal and opposite to said second phase shift (see figs. 4, 15, 24-25, 27-28 elements 141, 125, 235 and col.6, lines 41-58 and col.7, lines 9-30); and second section operable to facilitate combining (see fig.4 element 144 and col.7, lines 12-13) of said first and second adjusted signals.

As per claims 2, 8, teaches Obayashi et al wherein said second section includes transmitter (see fig.26 and col.22, lines 33-65) section which transmits first and second electromagnetic signals that respectively include said first and second adjusted signals.

As per claim 3, Obayashi et al teaches wherein said transmitter section includes first and second antenna elements which are physically spaced from each other, said first and second electromagnetic signals being respectively transmitted through said first and second antenna elements (see fig.26 and col.22, lines 33-65).

As per claims 4, 9 Obayashi et al teaches including filter section (see fig.4 element 124) which effects band-pass filtering said first analog signal before said first analog signal is supplied to said phase shift section, and which effects band-pass filtering said second analog signal before said second analog signal is supplied to said phase shift section

As per claims 5, 21 Obayashi et al inherently teaches, wherein said first and second digital signals each have a plurality of successive states, each of said states being selected one first second predetermined states which are different.

As per claims 6, 12, 22 Obayashi et al teaches wherein said first and second digital signals each have a plurality of successive states; wherein said digital-to-analog converter section generates for each said state of said first digital signal a respective corresponding pulse (see col.6, lines 8-21) of said first analog signal which has a duration less than the duration of the corresponding state, said digital-to-analog converter section outputting a predetermined voltage between successive said pulses of said first analog signal; and wherein said digital-to-analog converter section generates for each said state of said second digital signal a respective corresponding pulse of said second analog signal which has a duration less than the duration of the corresponding state, said digital-to-analog converter section outputting a predetermined voltage between successive said pulses of said second analog signal (see col.1, lines 5-65).

As per claim 10, Obayashi et al inherently teaches, wherein said predetermined voltage is approximately zero volt.

As per claim 11, Obayashi et al inherently teaches, wherein each said pulse has duration, which is approximately half the duration of the corresponding state of said digital signal.

As per claim 13, Obayashi et al inherently teaches wherein said digital-to-analog converter generates positive pulse having predetermined magnitude when the corresponding state of said digital signal is said first predetermined state, and generates

negative pulse having said predetermined magnitude when the corresponding state of said digital signal is said second predetermined state; wherein said predetermined voltage is approximately zero volts.

As per claim 14, Obayashi et al inherently teaches wherein each said pulse has duration, which approximately half the duration the corresponding states of said digital signal.

As per claim 15, Obayashi et al inherently teaches apparatus according each said pulse has approximately a square wave shape.

As per claim 24, Obayashi et al inherently teaches wherein said step generating pulses is carried out so that each said pulse has a duration which is approximately half the duration corresponding state said digital signal.

As per claim 25, Obayashi et al inherently teaches wherein said step of generating said digital signal is carried out so that each said state of said digital signal is a selected one of first and second predetermined states which are different.

As per claim 26, Obayashi et al inherently teaches, wherein said step of generating pulses includes the steps of generating positive pulse having a predetermined magnitude when the corresponding state of said digital signal is said first predetermined state, and generating a negative pulse having said predetermined magnitude when the corresponding state of said digital signal is said second predetermined state.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 16-19 and 27-28 are rejected under 35 U.S.C. 102(e) as being anticipate by Moriyama et al U.S. Patent No 6,091,941.

As per claims 16 and 27, Moriyama et al teaches apparatus, comprising: phase shifter is the same as the claimed (first section) which outputs first and second analog signals, said first analog signal representing predetermined waveform and said second analog signal representing substantially said predetermined waveform (see figs. 8-15 element 138 and col.14, lines 53-55); an orthogonal detector is the same as the claimed (first phase shift section) (see figs. 8-15 element 135 and col.14, lines 48-50) which produces first shifted signal by imparting to said first analog signal first phase shift, and which produces second shifted signal by imparting to said second analog signal second phase shift different from said first phase shift; an analog-to-digital converter section (see figs. 8-15 elements, 139-140 and col.14, lines 55-56) which converts said first and second shifted signals respectively into first and second digital signals; further phase shift section (see figs. 6-15 elements 24 or 113 and col.4, lines 15-27 and col.12, lines 52-col.13, lines 1-67) which produces a first adjusted signal by imparting to said first

digital signal phase shift which is substantially equal and opposite said first phase shift, and which produces second adjusted signal by imparting to said second digital signal phase shift which substantially equal and opposite to said second phase shift; and a second section operable to facilitate combining (see figs. 6-15, 28 element 28 or 118 and col.9, lines 44-46 and col.13, lines 56-59 and col.30, lines 29-35) of said first and second adjusted signals.

As per claim 17, Moriyama et al teaches a wherein said first section includes a receiver section (see 8-17). Furthermore implementing such receiver to have spaced antenna elements, and which receives substantially the same electromagnetic signal through each of said antenna elements, said first second analog signals each being derived from respective one of said antenna elements is inherently taught by Moriyama et al

As per claim 18, Moriyama et al teaches including filter section (see fig.8-17 element 134) which effect band pass filtering of said first shifted signal before said first shifted signal is supplied to said analog-to-digital converter section, and which effects band pass filtering of said second shifted signal before said second shifted signal is supplied to said analog-to-digital converter section.

As per claims 19, and 28 Moriyama et al teaches, wherein said first and second digital signals each have plurality successive states, each of said states being selected one of first and second predetermined states which are different (see figs. 8-17 elements 139-140).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ashara et al U.S. patent No 6,631,174 B1 teaches an automatic frequency control.

Maruyama U.S. Patent No 6,396,884 B1 teaches an automatic frequency control.

Sasaki U.S. Patent No 6,570,441 B1 teaches an incoherent demodulator.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vanderpuye Kenneth can be reached on 571 272 3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard
EMMANUEL BAYARD
PRIMARY EXAMINER

8/31/05